ABSTRACT OF THE DISCLOSURE

An orthogonal code generation apparatus can generate a sequence of orthogonal codes without having to prestore orthogonal code sequences in a memory, by applying logic operation on a sequence number and a location number using AND circuits A_0, A_1, A_2, A_3, $\cdots$, A_n and an adder circuit. A scrambling code generation apparatus computes only the values of registers involved with a feedback operation and a spreading operation, and loads respective values into the registers while shifting the shift register. When all the registers store valid values, scrambling codes are generated by a shift operation of the shift register.